Guidelines for MOSFET Device Optimization accounting for L-dependent Mobility Degradation

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Abstract

This paper reports a new methodology to monitor L-dependent mobility degradation based on empirical modeling of experimental results. This method allows benchmarking the impact on mobility degradation of different technological modules, thus giving some guidelines for device optimization.

Introduction

As channel length L of MOSFETs is scaling down, carriers' mobility μ is degraded by additional scattering mechanisms with a dramatic impact below 100nm. As reported by Andrieu *et al.* [1] and by Cros *et al.* [2] (Fig.1), this mobility crisis affects both electrons and holes. Moreover, this degradation has been measured for both poly-Si gate and metal gate [3], for both high-K and SiO_2 [4], for strained and unstrained devices [1,3], for doped and undoped channel [2,4] and also whatever the device architecture: Bulk [1], SOI, [4,5], Gate-All-Around [2] or FinFET [6]. This μ(L) degradation was confirmed whatever the extraction method, i.e. Y-function, Split-CV or magneto-resistance [7], and cannot be solely explained by ballistic effects [8,9]. Unfortunately, mobility falls is a sign of a poor quality of the transport in the channel keeping us away from the ballistic regime. Whatever the conduction regime (ballistic or drift-diffusion), the on-state current will be limited by a maximum velocity that can be expressed as $v_{lim} = \min(v_{sat},v_{inj})$ [10]. As shown in Fig.2, strong mobility degradation on short devices prevents from reaching the velocity limit, i.e. maximum on-current. Some authors [7,11] have identified those additional scattering mechanisms as impurity Coulomb scattering while neutral defects have been suggested by others [2,4]. This statement gives ground for a systematic examination of μ(L) degradation in order to establish guidelines for device optimization even if the precise origin of those additional scattering mechanisms is still not fully understood.

Extraction Methodology & μ-Degradation Modeling

A handy tool for extracting the mobility and monitoring its length dependence is the low field mobility $\mu_0=\mu_{eff}(Q_{inv}\approx 0)=\beta_0 C_{ox}^{-1} L_{eff} W_{eff}^{-1}$. β_0 at low V_{DS} ($<<V_{Dsat}$) is extracted from the Y-function [12] $Y(V_{GS})=I_D/g_m^{1/2}$ while effective channel length and width (resp. L_{eff} and W_{eff}) and gate oxide capacitance C_{ox} are obtained independently from gate-to-channel $C_{GC}(V_{GS})$ measurements [13]. The notion of μ_0 is illustrated by Fig.3. It is also worth noticing that classical Coulomb scattering and surface roughness terms do not significantly alter μ_0 at 300K. Using first order θ_1 and second order θ_2 mobility attenuation parameters, μ_{eff} in strong inversion can be reconstructed, showing good agreement in Fig.4 with R_{SD}-corrected split C-V extraction [14]. The use of μ_0 as a mobility indicator has been validated in Fig.5 by comparing it to split C-V extraction for different L_{eff}, clearly showing that μ_0 and μ_{eff} are degraded in similar way as L_{eff} is reduced. All our μ_0 extraction have been performed vs. L_{eff} to fairly compare the different technological splits. In order to construct our guidelines, we have introduced a new length dependent mobility degradation fitting model: $1/\mu_0(L_{eff})=1/\mu_{max}+\alpha_\mu/L_{eff}$. The two fitting parameters are the maximum mobility μ_{max} [$cm^2.V^{-1}.s^{-1}$], which is generally equal to the "long" channel mobility, and a mobility degradation factor α_μ [$nm.V.s.cm^{-2}$]. Fig.6 illustrates the different kinds of $\mu_0(L_{eff})$ curves that can be obtained, $\alpha_\mu=0$ meaning zero degradation and thus a constant μ_0. However, it should be noted that α_μ cannot be lower than its minimum value given by the ballistic mobility [15] $\alpha_{\mu bal}=(2kT/q)/v_{inj}$, v_{inj} being the injection velocity at source ($\alpha_{\mu bal}$ =0.04 or 0.08 $nm.V.s.cm^{-2}$ for electron and hole respectively).

Experimental Results

Gate stack: Gate stack impact on μ_0 was examined in Fig.7 & Fig.8. In Fig.7, two plasma nitrided SiON gate oxide thicknesses (12Å vs. 17Å) were compared for the same poly-Si gate, showing more degraded electron mobility for the thinner 12Å oxide. In Fig.8, we have found that nitrided metal gates (TiN, TaN) lead to more degraded electron mobility than the non-nitrided TaC metal gate. Those results are suggesting that N-species in the gate oxide and/or in the gate electrode lead to a lower long channel mobility in agreement with [16], but also to a higher α_μ i.e. to stronger scattering mechanisms.

Channel doping: Effect of channel doping was examined in Fig.9 using ultra thin body (UTB) structures in both cases (doped vs. undoped) for avoiding short channel effects disturbances. Devices fabricated using Silicon-On-Nothing (SON) technology have bulk S/D [17]. We found that increasing the channel doping is lowering the long channel electron mobility but has no significant effect on additional scattering mechanisms since close α_μ values were found.

Junction architecture: Since neutral defects introduction is likely related to the junction (S/D+LDD) ion implantation (I/I), S/D architecture appears as a key module for improving mobility degradation. Cros *et al.* have already shown in [2] that an increase of the temperature during the RTP activation anneal could cure partially the mobility degradation. Taking the problem differently, we have examined if it was possible to improve mobility degradation by changing I/I conditions (species, energy, dose). Results in Fig. 10 are demonstrating that S/D architecture optimization is possible even when reducing the RTP temperature.

Mobility boosters: After having examined some possible causes of degradation, we have now investigating the effects of mobility boosters on mobility degradation. Local process induced stress (PIS) engineering by using eSiGe stressors is studied in Fig.11, while surface orientation is considered in Fig.12. Even if both strategies have an impact on holes' μ_{max}, only local PIS which is also L-dependent [18] significantly improves α_μ.

Discussion & Guidelines

Seeing the strong degradation of the mobility, one could think that any mobility improvement is not relevant since all strategies will finally have the same mobility at very short gate length. Using our model, we have extrapolated from the measurements the resulting mobility at L_{eff}=10nm in Fig.13. We can see that mobility improvement is still possible even at 10nm if well optimized. We have also investigated a possible link between μ_{max} and α_μ in Fig.14: no clear correlation was found between the two parameters meaning that they are needed to monitor the mobility degradation. Thus we have introduced a new figure of merit $\eta=\mu_{max}/\alpha_\mu$. Higher η is, higher the short channel mobility will be and closer to its limiting velocity the device will operate. Finally, we give some guidelines, based on this work in Fig.15 in order to limit μ(L) degradation.

Conclusion

Using a new monitoring method based on empirical modeling of μ(L) degradation, we have systematically examined the impact on μ(L) of the gate stack, channel doping, junction architecture and mobility boosters. It has been found that this degradation is not ineluctable and that working on key technological modules would help us to get closer to the ballistic regime.

Acknowledgments

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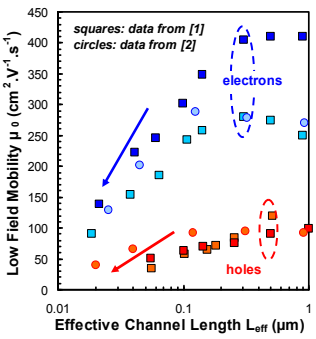

Fig.1: Literature data from [1] & [2] clearly showing length dependent mobility degradation for both electrons and holes.

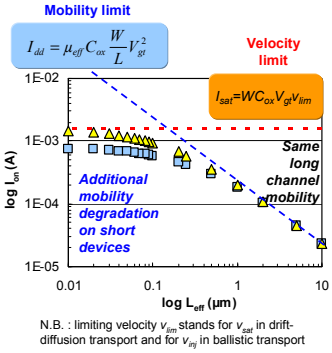

Fig.2: Strong mobility degradation on short devices prevents from reaching the velocity limit, i.e. maximum on-current.

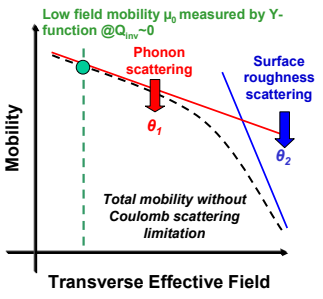

Fig.3: Illustration of low field mobility $\mu_0=\mu(Q_{inv}\approx 0)$. Coulomb scattering & surface roughness limitations are negligible.

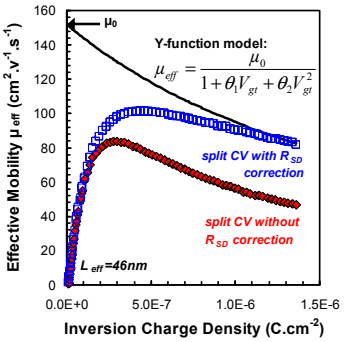

Fig.4: Series resistance R_{SD} correction which is critical on short devices is intrinsically taken into account when using Y-function.

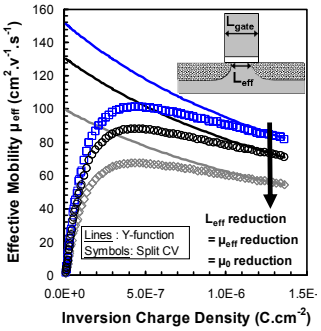

Fig.5: μ_{eff} measurements for different L_{eff}. θ_1 and θ_2 are kept constant for all channel lengths. Inset: L_{eff} definition

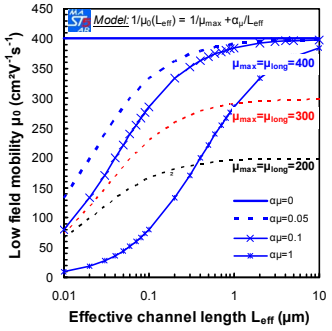

Fig.6: Length dependent mobility degradation model introducing mobility degradation factor α_μ. For $\alpha_\mu=0$, $\mu_0(L_{eff})$=Cte.

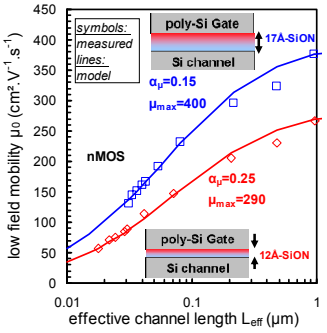

Fig.7: Comparison of electron mobility between two SiON gate oxide thicknesses. Thinner 12Å oxide is more degraded than 17Å.

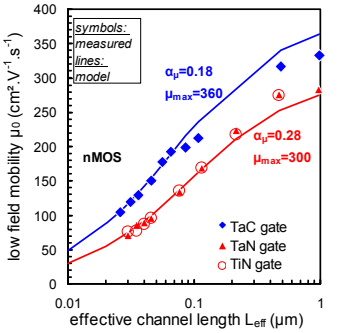

Fig.8: Comparison of electron mobility between different metal gate materials. Nitrided metals are more degraded than not nitrided.

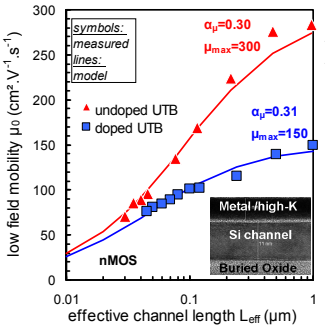

Fig.9: Comparison of electron mobility between undoped & doped ultra thin body (UTB) with high-K/metal gate stack.

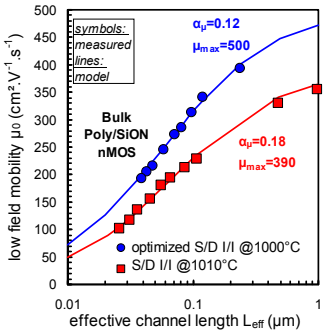

Fig.10: Comparison of electron mobility between two S/D architectures while keeping the same Poly/SiON gate stack.

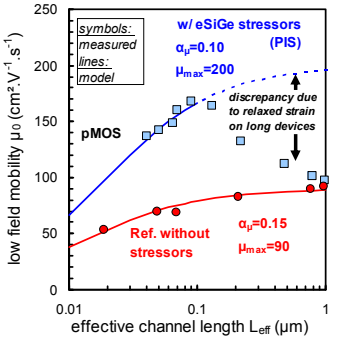

Fig.11: Comparison of hole mobility between unstrained reference and locally strained device with eSiGe S/D stressors.

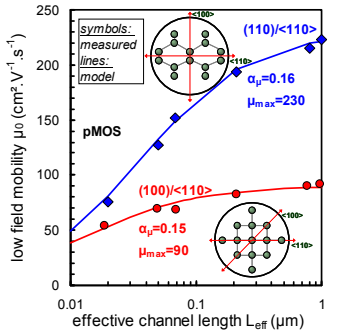

Fig.12: Comparison of hole mobility between (100)/<110> device and (110)/<110> device with same poly/SiON gate stack.

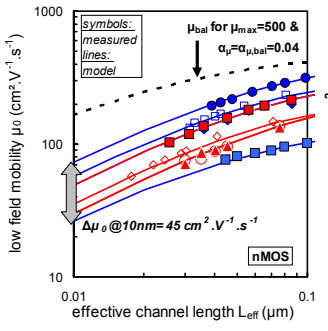

Fig.13: Sub-100nm electron mobility with extrapolation at L_{eff}=10nm using our model.

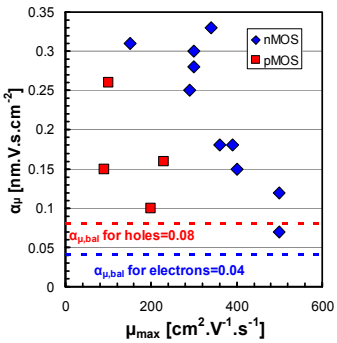

Fig.14: α_μ as a function of μ_{max} clearly showing no universal correlation between α_μ & μ_{max}.

Techno. module	impact on μ_{max}	impact on α_μ	η
Gate stack	+	++	x2 to x4
Junctions	+	+	x2
Channel doping	++	=	x2
Local PIS	++	+	x3
Crystal orientation	++	=	X2

Fig.15: Guidelines for short channel mobility optimization based on the figure of merit $\eta=\mu_{max}/\alpha_\mu$.

References

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